

REMARKS

Claims 1-12 are pending in this application. By this Amendment, the title and claim 1 is amended. Support for amended claim 1 may be found in the original specification at, for example, paragraph [0059] and FIG. 11. No new matter is added.

Applicant appreciates the courtesies shown to Applicant's representatives by Examiner Ma and Examiner Nguyen in the August 21, 2007 interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

Reconsideration of the application is respectfully requested.

Objection to the Specification

The title of the specification was objected to for allegedly being non-descriptive. The title is amended to overcome the objection. Accordingly, withdrawal of the objection to the specification is respectfully requested.

Claim Rejections

The following claims were rejected by the Patent Office:

claims 1-7, 9 and 12 under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 6,597,413 ("Kurashina");

claim 8 under 35 U.S.C. §103(a) as allegedly being unpatentable over Kurashina in view of U.S. Patent Publication No. 2006/0102903 ("Kim");

claim 10 under 35 U.S.C. §103(a) as allegedly being unpatentable over Kurashina in view of U.S. Patent Publication No. 2003/0202800 ("Matsushima"); and

claim 11 under 35 U.S.C. §103(a) as allegedly being unpatentable over Kurashina in view of U.S. Patent No. 6,480,244 ("Murade").

Applicant respectfully traverses each of the above rejections.

None of the applied references, alone or in combination, teach or suggest an electro-optical device including a substrate, data lines formed above the substrate and extending in a

predetermined direction and scanning lines formed above the substrate and extending in a direction intersecting the data lines, switching elements to which scanning signals are supplied from the scanning lines, pixel electrodes to which image signals are supplied from the data lines via the switching elements, an image display region defined as a region of the substrate in which the pixel electrodes and the switching elements are formed, a peripheral region defining the periphery of the image display region, a driver disposed in the peripheral region, exterior circuit connection terminals provided in the peripheral region at a position between the driver and a peripheral edge of the substrate, storage capacitors provided above the image display region to retain potentials of the pixel electrodes for a predetermined period of time, and a capacitor wire which supplies a predetermined potential to capacitor electrodes forming the storage capacitors and which is formed as the same film as that for electrodes forming the exterior circuit connection terminals, as recited in claim 1.

The Patent Office alleges that Kurashina discloses exterior circuit connection terminals provided above a peripheral region along a peripheral side of a substrate. Applicant respectfully disagrees.

The Patent Office alleges that scanning lines 3a (alleged exterior connection terminals) are provided above a peripheral region along a peripheral side of a substrate, which the Patent Office alleges is the area surrounding 9a and 30 of FIG. 7. That is, the Patent Office asserts that because the scanning lines 3a (alleged exterior connection terminals) of Kurashina travel to the exterior of an immediate circuit, it is an exterior circuit connection terminal. However, FIG. 7 clearly shows 3a to be in between 9a and 30, not in the area surrounding 9a and 30.

Further, Kurashina discloses that scanning line driving circuits 104, which are for driving the scanning lines 3a (alleged exterior connection terminals) by supplying thereto a scanning signal, are arranged on two sides of a first of a TFT array substrate 10 (see column

37, lines 12-15). That is, the scanning lines 3a (alleged exterior connection terminals) are connected to the scanning line driving circuits 104, and therefore the scanning lines 3a (alleged exterior connection terminals) cannot extend to the edge of the substrate. Thus, for at least this reason, the scanning lines 3a (alleged exterior connection terminals) of Kurashina are not exterior circuit connection terminals provided above the peripheral region along a peripheral side of a substrate, as required in claim 1.

Furthermore, the Patent Office alleges that Kurashina discloses a capacitor wire that supplies a predetermined potential to capacitor electrodes forming storage capacitors and that is formed as a same film as that for electrodes forming exterior circuit connection terminals, as required in claim 1. Applicant respectfully disagrees.

The Patent Office points to FIG. 1 and column 1, lines 37-40 of Kurashina for disclosing that scan lines (alleged exterior connection terminals) are formed as a same film as that of a capacitive line 11a (alleged capacitor wire). However, column 1, lines 37-40 is speaking of storage capacitors in the related art that contain scan lines, not external connection terminals as claimed. Further, at column 1, lines 52-65, Kurashina teaches away from electro-optical devices that have scan lines as the same film as capacitor wires stating that the electro-optical device suffers from cross-talk or ghosting in an image display, thereby degrading image quality. Furthermore, FIG. 7 of Kurashina, in contrast to the allegation made by the Patent Office that the scanning lines (alleged exterior connection terminals) are as the same film as capacitive line 11a (alleged capacitor wire), clearly shows that scan lines 3a (alleged exterior connection terminals) are not as the same film as capacitive line 11a (alleged capacitor wire). Not only are they each formed on different layers, they are each made of different materials as indicated by the shading of each in FIG. 7.

In addition, none of the applied references disclose a driver disposed in a peripheral region with exterior circuit connection terminals provided in the peripheral region at a

position between the driver and a peripheral edge of the substrate, as recited in claim 1. However, during the interview, Examiner Ma alleged that the location of a "peripheral region" was unclear. Applicant respectfully disagrees.

Claim 1 is clear in defining the location of the peripheral region. That is, as recited in claim 1, the peripheral region defines a periphery of an image display region and the image display region is defined as a region of a substrate in which pixel electrodes and switching elements are formed. Thus, claim 1 is clear in defining the location of the peripheral region with respect to the other features of the electro-optical device.

Further, none of Kim, Matsushima or Murade remedy the deficiencies of Kurashina in disclosing or rendering obvious the features of claim 1.

For at least the foregoing reasons, claim 1, and dependent claims thereof, are patentable over the applied references. As such, withdrawal of the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) is respectfully requested.

Double Patenting Rejection

The Patent Office rejected claims 1-12 over claims 1-21 of U.S. Patent Application No. 10/826,362 on the grounds of nonstatutory obviousness-type double patenting. Applicant respectfully traverses this rejection.

The 362 application has a later filing date than the above-identified application. In particular, the filing date of the 362 application is April 19, 2004. In contrast, the filing date of Applicant's application is April 12, 2004. MPEP §804 (I)(B)(1) recites "If a 'provisional' nonstatutory obviousness-type double patenting (ODP) rejection is the only rejection remaining in the earlier filed of the two pending applications, while the later-filed application is rejectable on other grounds, the examiner should withdraw that rejection and permit the earlier-filed application to issue as a patent without a terminal disclaimer."

Therefore, once all other rejections are overcome, the Examiner should withdraw the double patenting rejection and permit the earlier-filed application, i.e., the present application, to issue as a patent without a terminal disclaimer.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-12 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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